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Ohmic contacts with palladium diffusion barrier on III–V semiconductors

M. Galván-Arellano [a,*], J. Díaz-Reyes [b], R. Peña-Sierra [a]

[a] Depto. de Ing. Eléctrica, SEES, CINVESTAV-IPN, Apdo. Postal 14-740, México, D. F. 07000. Mexico
[b] CIBA-IPN, Ex-Hacienda de San Juan Molino, Km. 1.5, Tepetitla, Tlaxcala 90700, Mexico

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Ohmic contacts with a palladium (Pd) diffusion barrier were formed on GaAs substrates. The metal-contact structure consists of a gold-based-alloy/Pd/semiconductor-substrate. Characteristics of the deposited Pd films by "electroless" deposition on semiconductor-substrates are reported. SIMS analysis realized on the metal-semiconductor structures demonstrates the capability of the Pd films to act as a diffusion barrier. Contact resistance of the ohmic contacts was measured by the transmission line method (TLM).

1. Introduction

The III-V semiconductor technology is now a mature technology. III–V semiconductor devices find application in different technological areas. However, modern devices based on quantum well or super-lattice structures even require intensive research to develop suitable ohmic contacts. Ohmic contacts on modern devices must comprise very shallow regions of extension limited to few hundreds of nanometers. Good ohmic contacts must have contact resistance values of less than 10^{-5} Ω cm^2 [1]. The formation of shallow ohmic contacts presents several difficulties because of the huge quantity of physicochemical phenomena that happen at the metal–alloy interface [1]. Therefore, ohmic contacts on modern devices must include diffusion barriers in order to confine the contact extension.

In this study we will use GaAs substrates because of their wide use in III–V semiconductor technology. The main factors affecting the contact resistance of ohmic contacts are:

i) The physicochemical properties of the semiconductor (doping level and work function) and the surface characteristics (surface state density).
ii) The metal or metal-alloy selected to form the ohmic contact.
iii) The distinct processes applied to the semiconductor surface before the formation of the ohmic contact (it must include all the necessary stages to prepare the surface, such as the chemical-mechanical etching or the surface passivation processes).
iv) And the thermal annealing processes required to guarantee the electrical and mechanical stability of ohmic contacts.

There are various methods used for the fabrication of ohmic contacts. However, as a general rule a thermal annealing step is used for achieving contact integrity, therefore it is necessary to include this stage in any process to develop good ohmic contacts. The typical methods for ohmic contact formation on III-V semiconductor compounds can be summarized as follows:

A) The use of an interfacial degenerated thin film of the same semiconductor at the metal–semiconductor interface. The extension of the ohmic contact depends on the diffusion coefficient of the dopant and the chemical stability of the compounds formed at the interface.
B) Inclusion of an interfacial semiconductor–semiconductor heterojunction [2], with the lower-band gap semiconductor in contact with the metal. Typical examples are the GaAs ohmic contacts formed with an intermediate indium film. The annealing processes could produce films of InAs or $Ga_{1-x}In_xAs$ in close contact with the final gold metal-alloy. As the barrier produced at the lower-band gap semiconductor is minor, the contact resistance is greatly reduced.
C) Several kinds of ohmic contacts with diffusion barriers are reported in the literature. Some of these contacts are based on refractory metals such as tungsten, titanium or some noble metal based alloys, such as Pd–Ag and Pd–Au. Diffusion barriers with palladium (Pd) use films of ~10 nm thickness [1], however the reported results are incomplete to define the barrier functionality of the Pd films.

The preceding description refers to the general process for the ohmic contact formation. The entire process includes some wet steps applied at the semiconductor surface that unavoidably produce several metallic oxides, due to the use of water-based solutions or some other organic solvents. Therefore, it is necessary

* Corresponding author.
E-mail address: miguel_galvan_a@yahoo.com.mx (M. Galván-Arellano).

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